# PATENT SPECIFICATION

1,153,428

DRAWINGS ATTACHED.

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Int. Cl.:—**H 01 l 5/00.**

COMPLETE SPECIFICATION.

## Improvements in Semiconductor Devices.

We, MULLARD LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices.

In an article in the Proceedings of the Institute of Electrical and Electronic Engineers 1963 at page 1190 et. seq, by S. R. Hofstein and F. P. Heiman there is described a semiconductor device in which current flow in the surface of a semiconductor body is controlled by the voltage applied to an insulated gate electrode on the surface. Such a device is referred to as an insulated gate field effect transistor and consists of a monocrystalline semiconductor body of high bulk resistivity of one conductivity type having two low resistivity surface regions of the opposite conductivity type spaced apart in the body and forming two rectifying junctions with the bulk region of the body. A conductive layer is present on a dielectric layer on the surface of the body, with the conductive layer extending between the two surface regions. Ohmic contacts are made to the two low resistivity surface regions and the conductive layer. The dielectric layer may be produced by oxidation of the semiconductor body.

A voltage applied between the two surface regions biases one junction in the forward direction and the other junction in the reverse direction; the two surface regions are termed the source and drain regions, analogously to a junction type field effect device. Current flow between the two surface regions may be initiated and controlled by the voltage applied between the conductive layer, which is termed the gate electrode, and the source region. The voltage applied to the gate electrode is of such polarity that a surface channel of the opposite conductivity type is induced between the two surface regions under the dielectric layer and current flow occurs between the two surface regions through the induced surface channel. This mode of operation is referred to as the enhancement mode because the current carrying surface channel is formed by application of a voltage to the gate.

An insulated gate field effect transistor may be prepared which operates in the depletion mode; in this mode a current carrying channel is present at zero gate voltage and the concentration of charge carriers in the channel is decreased by application of a gate voltage of appropriate polarity. Such a device can also be operated in the enhancement mode by increasing the concentration of charge carriers in the channel. In the depletion mode the device is comparable to a junction field effect transistor in which the conductance of a current carrying channel is reduced by the depletion layer of a reverse biassed *P-N* junction. An insulated gate field effect transistor may be operated as a vacuum tube analogue with a modulating signal applied to the gate which has a high input impedance.

In operation the drain electrode is re-

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versed biassed and the depletion layer extends into the high resistivity substrate a greater distance than into the low resistivity drain region because of the lower concentration of charge carriers in the substrate. The wide depletion layer around the drain region causes the device to have a low output capacitance. The rate of change of depletion layer width (a) with source/drain voltage ($V_{DS}$) is high enough to cause the characteristics of the device to alter with the operating voltage to an undesirable extent for some applications. If a substrate of lower resistivity is used the rate of change

$$\left\{\frac{da}{dV_{DS}}\right\}$$

is reduced but the output capacitance is increased because of the narrower depletion layer. The minimum separation possible between the source and drain regions is limited by the variations in device characteristics with $V_{DS}$ and imposes on upper limit on the 'gm' obtainable with the device.

It is an object of the invention to provide a device in which a low output capacitance can be obtained together with a relatively small rate of change

$$\left\{\frac{da}{dV_{DS}}\right\}.$$

It is a further object of the invention to provide a device in which a relatively close spacing of source and drain regions can be obtained with a small rate of change

$$\left\{\frac{da}{dV_{DS}}\right\}.$$

According to the invention a semiconductor device comprises a monocrystalline semiconductor body having a high resistivity region of one conductivity type, two spaced surface regions of the opposite conductivity type at one side of the body forming the source and drain regions of an insulated gate field effect transistor, a dielectric layer on the surface of the body between the source and drain regions, a conductive gate electrode layer on the dielectric layer, ohmic contacts to the source and drain regions, an ohmic contact to the gate electrode layer, and a zone contiguous with the drain region having a concentration of active impurities such that in operation the width of the depletion layer extending into the material of the one conductivity type near the drain region in the vicinity of the said zone is less than the width of the depletion layer which would be formed in the absence of said zone.

In one form said zone consists of a layer of the one conductivity type which is contiguous with the drain region and extends towards the source region, said layer having a lower resistivity than the high resistivity region of the one conductivity type. The layer of the one conductivity type may extend between the source and drain regions and be contiguous with both of these regions. The layer of the one conductivity type may be situated between the high resistivity region of the one conductivity type and the dielectric layer. The layer of the one conductivity type may extend to a greater depth in the body than the source and drain regions.

The high resistivity region of the one conductivity type may be contiguous with a low resistivity surface region of the one conductivity type which is spaced from the source and drain regions of the opposite conductivity type and provides a low resistance contact to the depletion layer associated with the junction between the drain and the material of the one conductivity type when the device is in operation. In such a device the layer of the one conductivity type may extend to a greater depth in the body than the source and drain regions and be contiguous with the low resistivity surface region of the one conductivity type.

Between the layer of the one conductivity type and the dielectric layer there may be a second layer of the one conductivity type which is contiguous with the dielectric layer and with the first layer of the one conductivity type, the second layer having a resistivity which lies between the resistivity of said first layer and the resistivity of the high resistivity region of the one conductivity type.

In another form of a device in accordance with the invention said zone is of the opposite conductivity type, is contiguous with the drain region and extends in the direction of the source region, the zone having a concentration of active impurities characteristic of the opposite conductivity type which is lower than the concentration of active impurities characteristic of the one conductivity type in the adjacent high resistivity region of the one conductivity type. The zone of the opposite conductivity type may surround the drain region within the body and separate the drain region from the high resistivity region of the one conductivity type.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings in which:

Figures 1(a), 1(b) and 1(c) each show in a vtrtical section embodiments of a device according to the invention;

Figure 2 is an enlarged part of the vertical

sections of Figures 1(a) and (b) showing the positions of an inversion layer and a depletion layer which are formed in operation of the device;

Figure 3 shows vertical cross-sections of a semiconductor body at stages in the manufacture of the device shown in Figure 1(a);

Figure 4 shows a vertical section of an embodiment of which is a modification of the device shown in Figure 1(a);

Figure 5 shows a vertical section of another embodiment;

Figure 6 is an enlarged part of the vertical section of Figure 5 showing the position of a depletion layer which is formed in operation of the device;

Figure 7 shows vertical cross-sections of a semiconductor body at stages in the manufacture of the device shown in Figure 5;

Figures 8(a) and 8(b) show vertical sections of further embodiments; and

Figures 9(a) and 9(b) respectively show the depletion layer positions as a function of the applied field across the drain/substrate junction of a prior art device and a device as shown in Figure 8.

The device shown in Figure 1(a) comprises a resistivity $P$-type substrate 1 of monocrystalline silicon containing a boron concentration of approximately $10^{14}$ atoms. $cm^{-3}$. Two $N^+$-type surface regions 3, 4 containing phosphorus at a surface concentration of approximately $10^{20}$ atoms. $cm^{-3}$ are contiguous with the substrate and a surface layer 2 of $P$-type material containing boron at a concentration of approximately $10^{16}$ atoms $cm^{-3}$ is contiguous with the substrate 1 and the two regions 3, 4. The regions 3 and 4 each extend to a depth in the body of approximately $3\mu$ and the surface layer 2 extends to a depth of approximately $2\mu$. The distance between the $N^+$-type is $10\mu$ and the length of each region is 1mm. A dielectric layer 5 of silicon dioxide is present on the surface of the layer 2 and has a thickness $0.6\mu$. The layer 5 extends over the $P$-$N$ junctions between the $N^+$-type regions and the substrate. Ohmic contacts 8 and 7 to the regions and 3, 4 respectively are present, the contacts having been formed by evaporating aluminium through a mask. A conductive layer 6 of aluminium is present on the dielectric layer 5, the layer 6 having been formed simultaneously with the contacts 7 and 8. Electrical connections to the ohmic contacts 7, 8 and the conductive layer 6 are present.

In the device shown in Figure 1(b) the substrate consists of a $P^+$-type region 1A and a $P$-type layer 1B thereon. The spaced surface regions 3, 4 do not extend into the $P^+$-type region and the thickness of the $P$-type layer 1B is approximately $7\mu$ so that the regions 3, 4 are spaced from the $P^+$-type region 1A by approximately $4\mu$.

The region 1A has a boron concentration of $10^{17}$ atoms $cm.^{-3}$ and the layer 1B a boron concentration of $5\times10^{14}$ atoms $cm^{-3}$.

In the device shown in Figure 1(c) the $P$-type region 38 in which the current carrying channel is formed extends beyond the $N^+$-type surface regions 41, 42 to and is contiguous with, the $P^+$-type region 37. The $P^-$-type region parts 39, 40 may be regarded as the remnant of the $P$-type layer 1B of Figure 1(b) as the $P$-type layer 2 is moved down to extend to the $P^+$-type region 1A.

The boron concentrations in the various regions are:

| | | |
|---|---|---|
| $P$-type | (38) | $10^{16}$ atoms. $cm.^{-3}$ |
| $P^+$-type | (37) | $10^{17}$ atoms. $cm.^{-3}$ |
| $P^-$-type | (39, 40) | $5\times10^{14}$ atoms. $cm.^{-3}$ |

Referring now to Figure 2, in operation the drain region 3 is made positive with respect to the source region 4, a positive voltage is applied to the conductive layer 6 constituting the gate electrode to form an $N$-type inversion layer in the surface layer 2. The inversion layer is delineated by the chain line 11. The $P$-$N$ junction between the drain region 3 and the substrate 1 is reverse biassed and the depletion layer extends into the substrate 1 to a distance shown by the dotted line 9 and into the surface layer 2 to a position shown by the dotted line 10.

There is a further depletion layer under the inversion layer 11, but this is not shown for reasons of clarity. The extension of the depletion layer into the surface layer 2 is less than the extension into the substrate 1 because of the higher concentration of charge carriers in the surface layer 2. Current flows between the source and drain through the inversion layer and part of the depletion layer in the surface layer. The device has an output capacitance almost as low as a device without a surface layer 2 but the rate of change

$$\left\{\frac{da}{dV_{DS}}\right\}$$

is relatively low because this parameter is determined by the doping in the depletion layer through which the current flows. The device may be used in the usual applications for insulated gate field effect transistors.

The region 1A of the device shown in Figure 1(b) provides a low resistance path to the depletion layer surrounding the drain surface region and the current carrying channel: this reduces the power loss at high frequencies in the internal impedance between the drain surface region and the substrate.

In the device shown in Figure 1(c) the extension of the region 38 of relatively low resistivity to contact the $P^+$-type region 37 provides a low resistance path for capacitive current between the current carrying channel and the $P^+$-type region 37 and reduces the power loss at high frequencies.

The manufacture of the transistor shown in Figure 1(a) will now be described with reference to Figure 3. A substrate 1 of high resistivity monocrystalline silicon containing boron at a concentration of $10^{14}$ atoms cc.$^{-3}$ had a layer of silicon 2 epitaxially grown on one surface to a depth of $2\mu$; this surface layer contained boron at a concentration of $10^{16}$ atoms cm.$^{-3}$. This layer could alternatively be formed by the diffusion of boron into the substrate. A layer of silicon dioxide of $0.6\mu$ thickness is grown on the surface layer 2 by oxidation in wet nitrogen at 1200°C for 30 minutes. Windows are then opened in the silicon dioxide layer using conventional photolithographic techniques and phosphorus is diffused through the windows to give two $N^+$-type surface regions 3, 4 having a surface concentration of phosphorus of $10^{20}$ atoms. cm.$^{-3}$. The structure at this stage is shown in Figure 3(b).

Aluminium layers 6, 7 and 8 are deposited on the silicon dioxide layer 5, the surface region 4 and the surface region 3 respectively (Figure 3(c) Deposition of aluminium is effected through a mask and the thickness of the layers 6, 7 and 8 is $0.3\mu$. Electrical connections are made to each of the aluminium layers 6, 7 and 8.

The device shown in Figure 4 is a modification of the device shown in Figure 1 in that the $P$-type surface layer 12 only extends a certain distance from the drain surface region 13. The surface layer 12 extends $3\mu$ from the drain surface region towards the source surface region. With a spacing of less than $10\mu$ between the source and drain regions, the surface layer may extend less than $3\mu$ from the drain surface region. The concentration of boron in the surface layer 12 is $10^{16}$ atoms. cm.$^{-3}$ and may be formed by diffusion through a masking oxide layer which has been defined using photoresist techniques. In operation this device is similar to the device shown in Figure 1; the depletion layer is narrower in the surface layer 2 and the depletion layer has a contour similar to that of the depletion layer shown at 9, 10 in Figure 2.

The device shown in Figure 5 comprises a high resistivity substrate 14. Two $N^+$ surface regions 15, 16 extend into the substrate from one surface thereof. A buried $P$-type layer 17 having a lower resistivity than the substrate 14 extends between the surface regions 15, 16. Between the buried layer 17 and a dielectric layer 18 there is a thin $P$-type surface layer 19 of high resistivity material. The thickness of the surface layer 19 is $1\mu$ and the width of the buried layer 17 is $2\mu$, the $N^+$-type surface regions are formed by diffusion and extend to a depth of $4\mu$ in the substrate 14. The device may be prepared by epitaxial techniques similar to those described for the device shown in Figure 1.

The manufacture of the device shown in Figure 5 will now be described with reference to Figure 7.

In Figure 7(a) there is shown a microcrystalline silicon body 20 of $P$-type conductivity containing boron at a concentration of $10^{14}$ atoms. cm$^{-3}$ and having a hole 21 formed in one surface by ultrasonic means. The hole has a depth of $5\mu$ and a width of $15\mu$. Using epitaxial techniques a layer 22 of $P$-type silicon with a concentration of boron of $10^{16}$ atoms. cm.$^{-3}$ and a layer 23 of $P^-$-type silicon with a concentration of boron of $10^{14}$ atoms. cm$^{-3}$ are deposited on the monocrystalline substrate 20 to yield the structure shown in Figure 7(b). The epitaxial layers are then ground away down to the chain line shown in Figure 7(b) using Alumina of approximately $0.5\mu$ particle size to give the surface structure shown in 7(c). Phosphorus is then diffused into the surface of the silicon body through openings in an oxide masking layer to form $N^+$-type diffused regions 24. 25 which have a surface concentration of phosphorus of $10^{20}$ atoms. cm.$^{-3}$

In operation of the device the junction between the drain region 16 and the $P$-type regions 14, 17, 19 is reverse biassed. Due to the relatively higher concentration of charge carriers in the buried layer 17 the depletion layer indicated by the dotted line 26 in Figure 6 extends a shorter distance into this region than into the substrate 14. The depletion layer at the surface between the surface layer 19 and the dielectric 18 is narrower than the depletion layer in the substrate 14 as shown in Figure 6.

The device shown in Figure 8(a) comprises a $P$-type substrate 27 having a boron concentration of $10^{16}$ atoms. cm.$^{-3}$, regions 28, 29 on one surface, the region 29, intended as the drain region being formed in an $N$-type region 30 having a concentration of phosphorus of $10^{14}$ atoms. cm.$^{-3}$. The region 30 has been formed by epitaxial deposition in an ultrasonically drilled hole in the substrate 27.

Figure 9(a) shows the extension of the depletion layer associated with the drain/substrate junction of a prior art device in which the doping on the drain side of the junction is $10^{20}$ donor atoms. cm.$^{-3}$ and on the substrate side of the junction is $10^{14}$ acceptor atoms cm$^{-3}$. Due to the lower doping in the $P$-type substrate the volume of the depletion layer in the substrate is much greater than

in the drain region. Figure 9(b) shows the extension of the depletion layer associated with the junction between the *N*-type region 30 and the *P*-type substrate 27 of the device shown in Figure 8(a). Due to the higher doping on the *P*-type substrate side of the junction 33 ($10^{16}$ atoms. $cm^{-3}$) than on the *N*-type side of the junction 33 ($10^{14}$ atoms $cm.^{-3}$), the volume of the depletion layer in the substrate is much less than the volume of the depletion layer in the *N*-type region 30. The output capacitance of the device is dependent upon the width of the depletion layer enclosing the reverse biassed *P-N* junction 33. As previously mentioned the width of the depletion layer is dependent on the applied field. With a device having high resistivity substrate as shown in Figure 9(a) the distance x through which the edge of the depletion layer 35 moves for a change dV in the applied field is larger than the distance y through which the edge of the depletion layer 36 of the device shown in Figure 9(b) moves for the same change dV in the applied field. Thus the rate of change

$$\left\{\frac{da}{dV_{DS}}\right\}$$

is less for the configuration shown in Figure 9(b) than for the configuration shown in Figure 9(a).

Thus the characteristics of the device are made less dependent upon the voltage $V_{DS}$ applied to the device. The gate electrode in the device illustrated in Figure 8(a) extends over the *P-N* junction between the substrate 27 and the region 30, which has a width of $3\mu$ between the region 29 and the substrate 27.

The region 30 may be formed only at the surface of the substrate 27 and extending between the surface region 29 and under the gate electrode. In this case the output capacitance would not be decreased to such an extent as when the region 30 surrounds the region 29 and separates this region from the substrate 27, as shown in Figure 8(a) but a relatively low output capacitance is still obtained. Such an arrangement of the regions is shown in Figure 8(b) in which the region 30 is seen to extend between the region 29 and the substrate 27 only at the surface of the substrate.

In Figure 5 the buried layer 17 may only extend $3\mu$ from the drain region 16. Although this embodiment may be difficult to prepare the effective section of the buried layer 17 is retained and in operation the device would have similar characteristics to the device illustrated in Figure 5. The distance which the buried layer extends from the drain is not critical provided the depletion layer is always within the buried layer during operation.

The device shown in Figure 8 may have a region extending from the drain region towards the source region as illustrated in Figures 1, 4 or 5. In this embodiment the substrate has an acceptor concentration of $10^{16}$ atoms. $cm.^{-3}$ and a thin surface layer with a depth of $1\mu$ has a concentration of $10^{14}$ atoms. $cm.^{-3}$ and extends between the source and drain regions. The depletion layer in the thin surface layer is displaced in a manner similar to that shown for the depletion layer 26 in Figure 6 due to the higher charge concentration in the substrate.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a monocrystalline semiconductor body having a high resistivity region of one conductivity type, two spaced surface regions of the opposite conductivity type at one side of the body forming the source and drain regions of an insulated gate field effect transistor, a dielectric layer on the surface of the body between the source and drain regions, a conductive gate electrode layer on the dielectric layer, ohmic contacts to the source and drain regions, an ohmic contact to the gate electrode layer, and a zone contiguous with the drain region having a concentration of active impurities such that in operation the width of the depletion layer extending into the material of the one conductivity type near the drain region in the vicinity of the said zone is less than the width of the depletion layer which would be formed in the absence of said zone.

2. A semiconductor device as claimed in Claim 1, wherein said zone consists of a layer of the one conductivity type which is contiguous with the drain region and extends towards the source region, said layer having a lower resistivity than the high resistivity region of the one conductivity type.

3. A semiconductor device as claimed in Claim 2, wherein the layer of the one conductivity type extends between the source and drain regions and is contiguous with both of these regions.

4. A semiconductor device as claimed in Claim 2 or Claim 3, wherein the layer of the one conductivity type is situated between the high resistivity region of the one conductivity type and the dielectric layer.

5. A semiconductor device as claimed in any of Claims 2 to 4, wherein the layer of the one conductivity type extends to a greater depth in the body than the source and drain regions.

6. A semiconductor device as claimed in any of Claims 2 to 5, wherein the high resistivity region of the one conductivity type is contiguous with a low resistivity surface region of the one conductivity type which is

spaced from the source and drain regions of the opposite conductivity type and provides a low resistance contact to the depletion layer associated with the junction between the drain region and the material of the one conductivity type when the device is in operation.

7. A semiconductor device as claimed in Claims 5 and 6, wherein the layer of the one conductivity type extends to and is contiguous with the low resistivity surface region of the one conductivity type.

8. A semiconductor device as claimed in any of Claims 2 to 7, wherein between the layer of the one conductivity type and the dielectric layer there is a second layer of the one conductivity type which is contiguous with the dielectric layer and with the first layer of the one conductivity type, the second layer having a resistivity which lies between the resistivity of said first layer and the resistivity of the high resistivity region of the one conductivity type.

9. A semiconductor device as claimed in Claim 1, wherein said zone is of the opposite conductivity type, is contiguous with the drain region and extends in the direction of the source region, the zone having a concentration of active impurities characteristic of the opposite conductivity type which is lower than the concentration of active impurities characteristic of the one conductivity type in the adjacent high resistivity region of the one conductivity type.

10. A semiconductor device as claimed in Claim 9, wherein the zone of the opposite conductivity type surrounds the drain region within the body and separates the drain region from the high resistivity region of the one conductivity type.

11. A semiconductor device substantially as herein described with reference to and as illustrated in Figure 1(a), Figure 1(b), Figure 1(c), Figure 4, Figure 5 or Figure 8 of the accompanying drawings.

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FIG. 1.

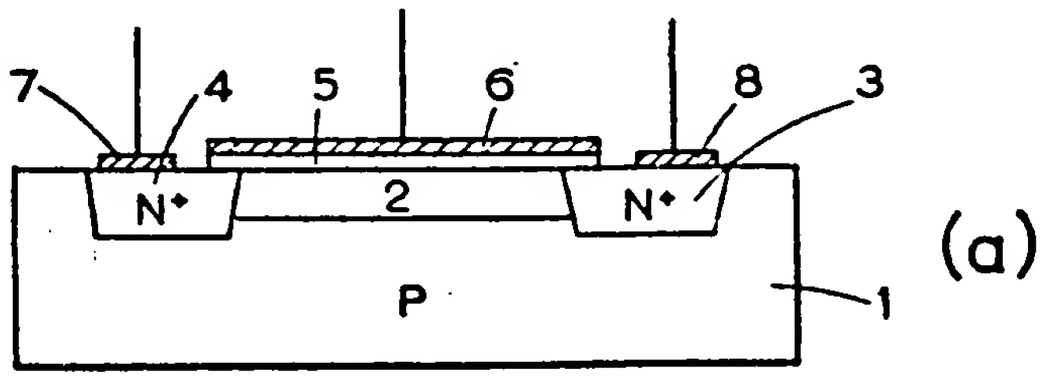


FIG. 2.

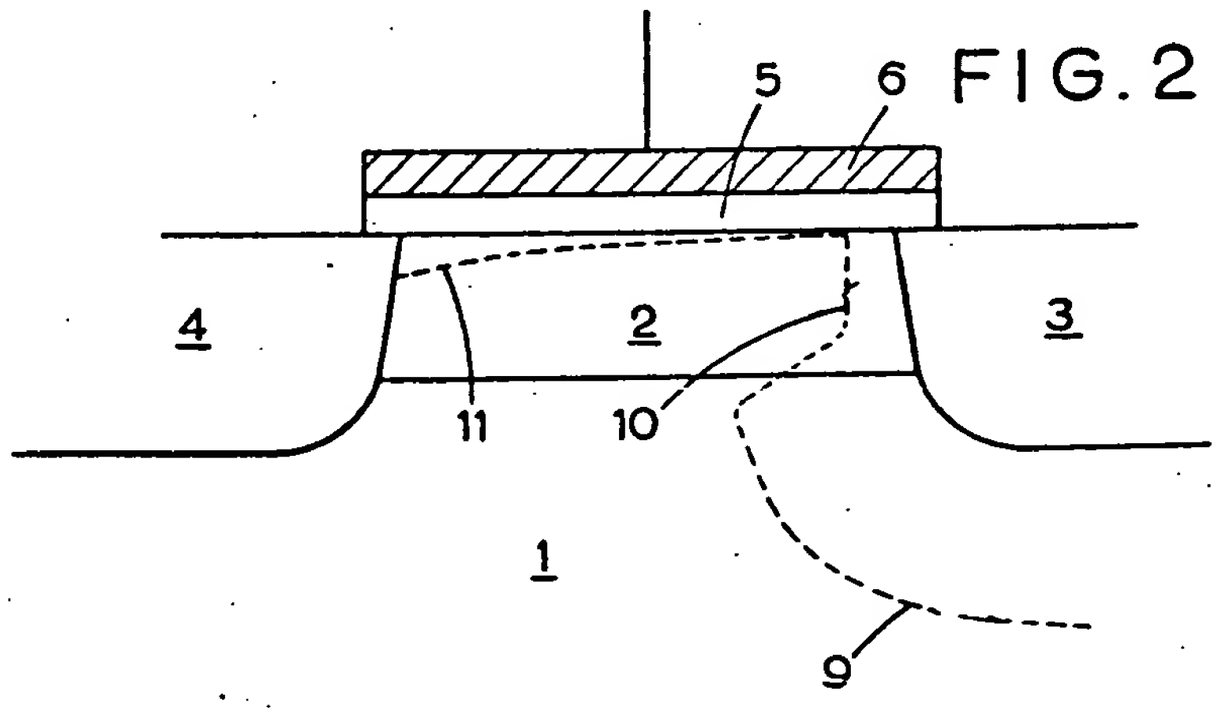

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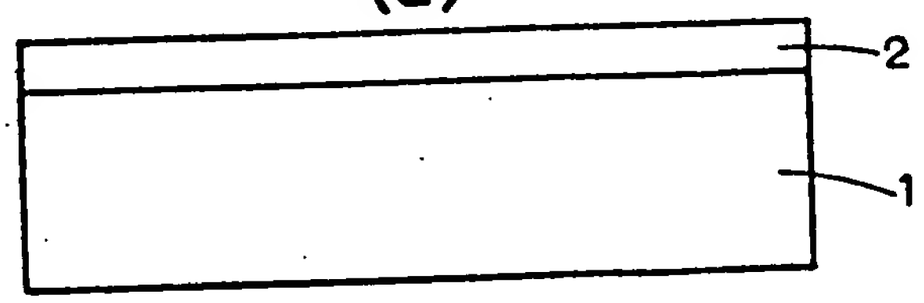
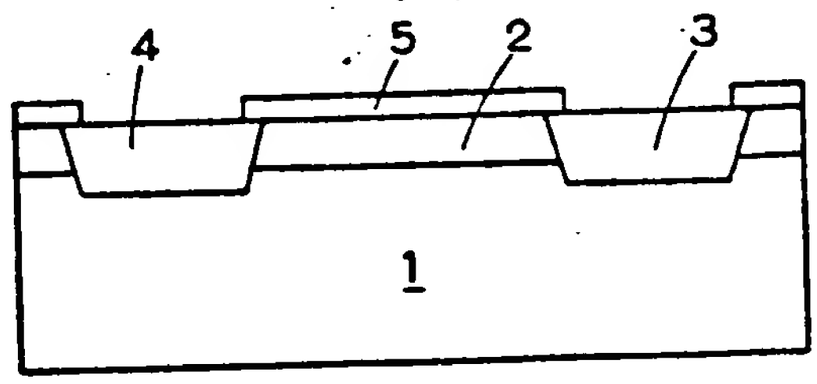
FIG.3.

(a)




(b)




(c)

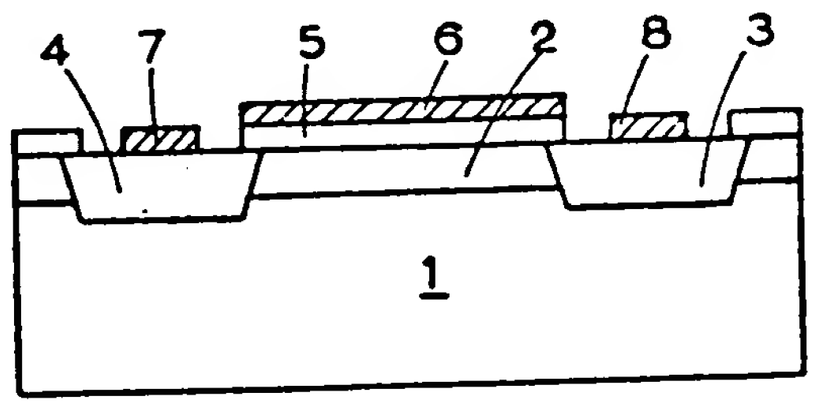


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FIG. 4.

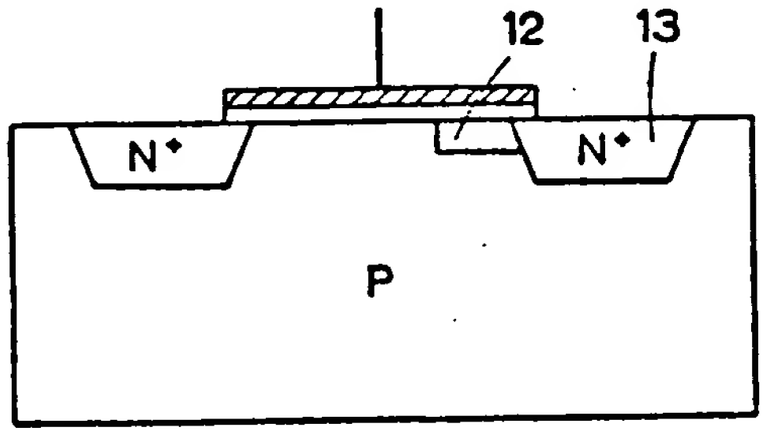


FIG. 5.

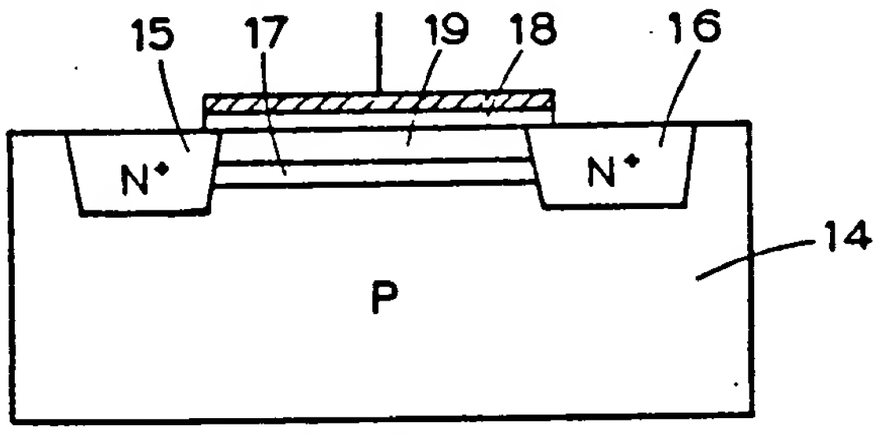


FIG. 6.

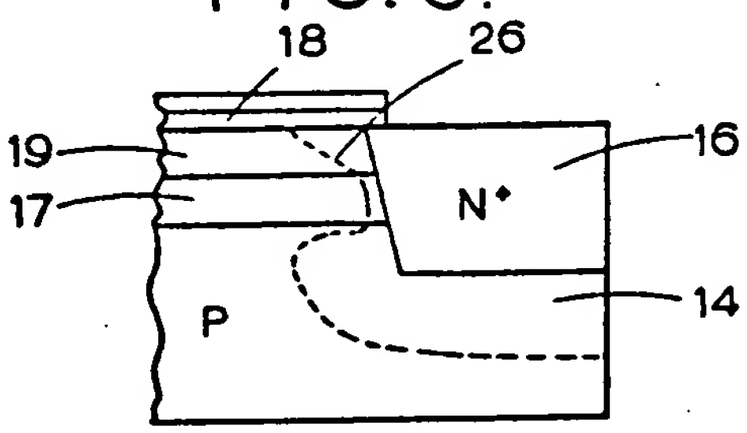

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FIG. 7.

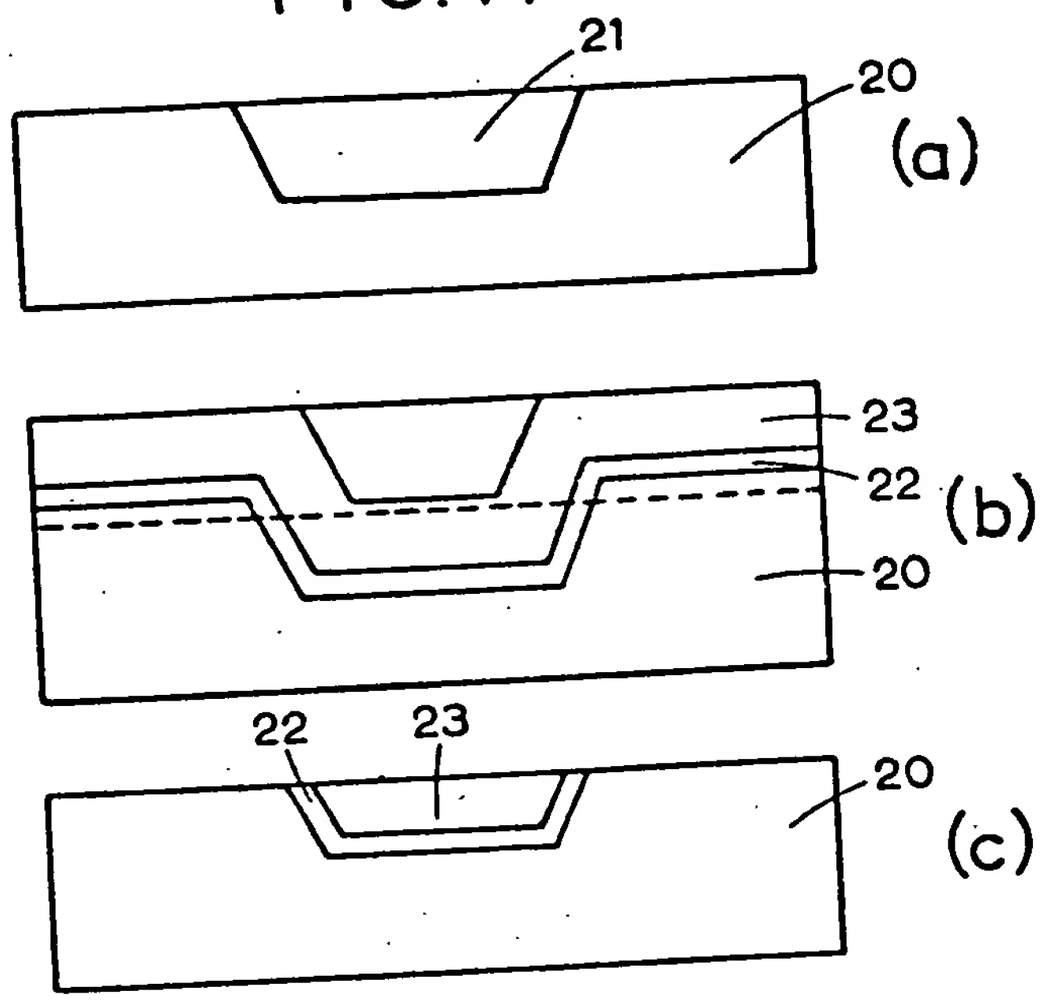
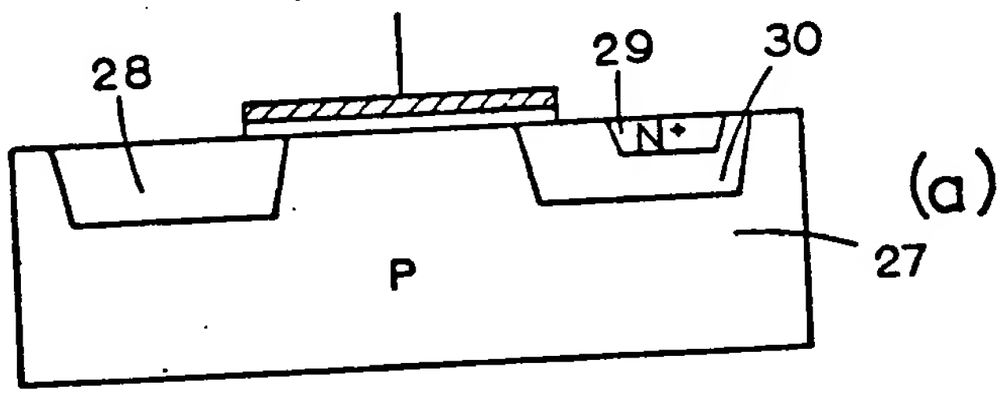



FIG. 8.



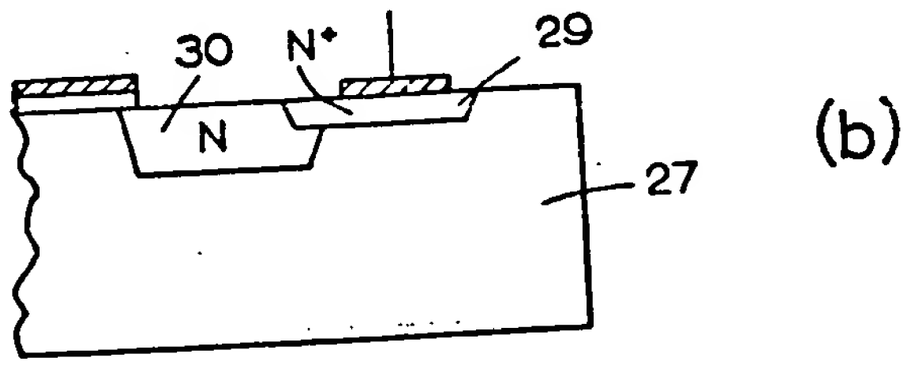



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FIG. 9.